UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,890	08/20/2003	Hee-Choul Lee	4234-13	8184

20575 7590 02/18/2009

MARGER JOHNSON & MCCOLLOM, P.C.
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204

EXAMINER	
RUTKOWSKI, JEFFREY M	
ART UNIT	PAPER NUMBER
2419	

MAIL DATE	DELIVERY MODE
02/18/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/645,890	LEE, HEE-CHOUL	
	Examiner	Art Unit	
	JEFFREY M. RUTKOWSKI	2419	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 November 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 11/20/2008 are accepted.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. **Claims 1-21 and 23-26** are rejected under 35 U.S.C. 103(a) as being unpatentable over Thorson (US Pat 5,533,198) in view of Passint et al. (US Pat 6,230,252), hereinafter referred to as Passint in view of Admitted Prior Art, hereinafter referred to as APA.

6. For **claim 1**, Thorson discloses a multi-dimensional broken mesh network, where each node is one or more processors (input/output protocol processing links connected to the broken links) **[col. 4 line 59, figure 1]**. Coordinates are used to define how information moves from a start node (starting switching element) to a destination node (ending switching element) **[col. 6**

lines 16-20]. If any of the links are broken between nodes, communication is restored by changing the direction of the information flow in a plus or minus direction **[col. 5 lines 55-58]**.

7. Thorson discloses the use of processors (input/output protocol processors) in a mesh network. It is not clear from the teachings of Thorson if there are external links connected to the processors. Passint discloses a mesh network where router chips **0-7** (input/output protocol processors) all reside on the boundary of the mesh network and have external links **[figure 5]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Passint's topology in Thorson's invention to provide a scalable system **[Passint, abstract]**.

8. Thorson discloses the use of a multi-dimensional mesh network where each processing node has a set of coordinates **[figure 1]**. Thorson's disclosure is not clear how many tuples are used to identify a coordinate. The APA discloses that conventional mesh networks have n tuple coordinates. Additionally, each element has n-1 same coordinates and a different coordinate of plus minus 1 **[0053]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use n-tuple coordinates in Thorson's invention to provide a way to find a processing unit from any location in the mesh.

9. Thorson does not disclose a processing element that performs protocol conversion. The APA discloses a switching network that makes use of protocol conversion to transport information **[0014]**. It would have been obvious to a person of ordinary skill in the art to perform protocol conversion in Thorson's invention to provide self-routing functionality.

10. The combination of Thorson and the APA disclose the use of n-tuple coordinates. It is not clear from the teachings of the combination if the coordinates are numbered in an increasing way. Passint discloses a network that transmits packets of information between the processor

nodes in the + and - directions of three dimensions and routes packets toward two nodes, which both include four processors. In other words, one router chip 50 communicates directly with eight processors (130, 131,132, 133, 130', 131', 132', and 133') **[col: 6, lines: 65-68, figures 3 and 19A]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use increasing coordinates in Thorson's network to increase fault tolerance.

11. For **claim 2**, Thorson discloses a processing element that is made up of one or more processors **[col. 8 lines 34-37 and figure 5]**.

12. For **claims 3, 5-6**, Thorson discloses a multi-dimensional broken mesh network, where each node can be one or more processors (input/output protocol processors) **[col. 4 line 59, figure 1]**. Thorson does not disclose the use of jumping routes. Passint discloses a network where diagonal routes (jumping routes) are used to interconnect elements **[figure 5]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use jumping routes in Thorson's network to increase fault tolerance.

13. For **claim 4**, Thorson does not disclose the use of a control system bus. Passint discloses a system control bus that interconnects two processors **30, 32 [figure 1]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a system control bus in Thorson's network to increase fault tolerance.

14. For **claim 7**, Thorson discloses coordinates are used to define how information moves from a start node (starting switching element) to a destination node (ending switching element) **[col. 6 lines 16-20]**. If any of the links are broken between nodes, communication is restored by changing the direction of the information flow in a plus or minus direction **[col. 5 lines 55-58]**.

15. For **claim 8**, Thorson does not disclose elements having n-1 same coordinates and the different coordinate different by 1. The APA discloses that conventional mesh networks are have n tuple coordinates. Additionally, each element has n-1 same coordinates and a different coordinate of plus minus 1 **[0053]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use n-tuple coordinates in Thorson's invention to provide a way to find a processing unit from any location in the mesh.

16. For **claims 9-12**, Thorson does not disclose the use of jumping routes. Passint discloses a network where diagonal routes (jumping routes) are used to interconnect elements **[figure 5]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use jumping routes in Thorson's network to increase fault tolerance.

17. For **claim 13**, Thorson discloses the use of an input buffer with an input buffer monitor and an output buffer **[col. 4 lines 62-63, col. 8 lines 55-57 and figure 5]**.

18. Thorson does not disclose the use of a switching controller. Passint discloses a router chip **50** (switching controller) examines a sideband to determine which virtual channel buffer the message belongs in **[col. 16 lines 41-43]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a switching controller in Thorson's network to control congestion **[Passint, col. 16 lines 43-44]**.

19. For **claim 14**, Thorson discloses the use of an input buffer with an input buffer monitor and an output buffer **[col. 4 lines 62-63, col. 8 lines 55-57 and figure 5]**. Thorson does not disclose the use of an output buffer monitor. Passint discloses a router chip **50** (output buffer monitor) examines a sideband to determine which virtual channel buffer the message belongs in **[col. 16 lines 41-43]**. It would have been obvious to a person of ordinary skill in the art at the

time of the invention to use a switching controller in Thorson's network to control congestion **[Passint, col. 16 lines 43-44]**.

20. For **claim 15**, Thorson discloses if a node **42.18** wants to send a message to node **42.17**, it would access the look-up table for the stored (buffered) entry stored for corresponding to node 42.17 **[col. 9, lines 22-25 and col. 10 lines 44-46]**.

21. For **claim 16**, Thorson does not disclose the use of dynamic self-routing. Passint discloses a routing scheme where global routing and local routing are used to provide routing information dynamically as they pass through network **[col. 11 lines 15-18]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use dynamic routing in Thorson's network to increase fault tolerance.

22. For **claim 17**, Thorson does not disclose packet discard techniques. Passint discloses a router receives block **102**, accepts data includes virtual channel management for keeping or discarding data **[col. 11 lines 10-13]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use discard techniques in Thorson's network to increase fault tolerance.

23. For **claim 18**, Thorson does not disclose the use of FIFO discard. Passint discloses a router receives block 102, accepts data includes virtual channel management, dynamically allocating memory queues similar to First-In First-Out (FIFO) for keeping or discarding data **[col. 11 lines 10-13]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use FIFO discard techniques in Thorson's network to increase fault tolerance.

24. For **claims 19 and 20**, Thorson discloses the use of n-tuple delta values by disclosing a situation where the link between nodes 12.14 and 12.11 is rendered inoperable, communication is still possible simply by changing the direction ordering so as to change the occurrence of the -y move. In that case, the direction order routing method could be chosen as (+x, -y, z, -x, +y, -z) and the packet to be transferred between node 12.7 and node 12.11 will be transferred from node 12.7 to node 12.8 and then through nodes 12.5 and 12.2to node 12.11 **[col. 5 lines 63-67]**.

25. Specifically for **claim 20**, Thorson discloses the use of processors connected to memory **[col. 8 lines 36-38, figure 5]**.

26. For **claims 21 and 23-24**, Thorson does not disclose the use of switching elements mounted on a switching board. Passint discloses routers that are mounted on circuit boards **[col. 9 lines 17-18]**. Figure 10 if Passint suggests using wiring to interconnect the routers. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use Passint's arrangement in Thorson's network to increase fault tolerance.

27. For **claim 25**, Thorson discloses a mesh network that has n-dimensionally arranged frames; n-dimensional unit cells defined by n-tuple frames of each dimension **[Figure 1]**.

28. Thorson discloses the use of processors **[col. 4 line 59, figure 1]**. Thorson does not disclose a processing element that performs protocol conversion. The APA discloses a switching network that makes use of protocol conversion to transport information **[0014]**. It would have been obvious to a person of ordinary skill in the art to perform protocol conversion in Thorson's invention to provide self-routing functionality.

29. Thorson does not disclose the use of switching boards mounted in a unit cell. Passint discloses a router board that includes four routers (switching boards mounted in unit cell) **[figure**

5]. It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate and establishing a method for routing a packet between a source and a destination node in a network system with n-dimensional topology in Thorson's invention to increase fault tolerance.

30. For **claim 26**, Thorson does not disclose unit cells that do not have the switching board. Passint discloses routers **1 and 3** do not have switching boards **[figure 10]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to uses routers that do not have switching boards in Thorson's invention to increase fault tolerance.

31. **Claims 22 and 27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Thorson in view of Passint and the APA as applied to **claims 21 and 25 respectively** above, and further in view of Brock et al. (US Pat 6,836,849), hereinafter referred to as Brock.

32. For **claim 22**, the combination of Thorson, Passint and the APA do not disclose the use of a cooling flow. Brock discloses the use of a cooling fan **322** and a solid state cooling device **323 [figure 3]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use cooling fans in Thorson's invention to keep elements from overheating.

33. For **claim 27**, the combination of Thorson, Passint and the APA do not disclose the use of a guide means. Brock discloses a guide means by showing a multiprocessor system **304** that is inserted into the slot of rack **301 [figure 1]**. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a guide means in Thorson's invention to interconnect different elements.

Response to Arguments

34. The argument with respect to Thorson not disclosing a broken mesh network is not persuasive because the claims do not require an architecture where there are no direct connections between local traffic sources or sinks and the switching elements. For example, if there are four switching elements connected in a mesh. If the links between the switching elements are broken and I/O processors are connected to the broken links, it appears the processors have replaced the switching elements in the architecture and are now connected in a mesh. The Examiner views this as being reasonable because there is no requirement to connect the switching elements to the I/O processors in a particular arrangement.

35. The argument with respect to Thorson and Passint not disclosing or suggesting breaking connections between starting and ending switching elements is not persuasive. Since Thorson's invention could be applied to any k-ary n-cube mesh **[col. 4 lines 55-58]**, this suggests the breaking of connections by the switching elements to form a different type of mesh by modifying the dimensions of the cube. Passint also suggests the disconnecting of connections by disclosing, in figures 4-5 and 10, the different architectures that can be used in Passint's invention.

36. The argument with respect to Passint not disclosing protocol conversion is not persuasive because this feature was cited as being taught by the APA.

37. The argument with respect to Passint not disclosing external traffic links is not persuasive because figure 5 of Passint discloses the use of external links via **PP** interfaces.

38. The argument with respect to the motivation to combine Thorson and Passint is not persuasive. The Examiner agrees with the Applicant that Thorson is already scalable to only a certain degree. Thorson's invention does not disclose the interconnection of elements in a mesh

(cube) but not a full mesh (hypercube). Passint provides a more scalable system than Thorson by expanding the mesh topology to a full mesh topology (hypercubes).

39. The argument with respect to the structural differences between Thorson and Passint could render the combination unsatisfactory is not persuasive. It is not clear how the Applicant feels modifying Thorson with Passint renders Thorson's invention unsatisfactory for its intended purpose.

40. The arguments with respect to the motivation to combine Thorson and the APA are not persuasive because the portion of Thorson cited by the Applicant discusses the use of a look-up table to select paths. The cited portion does not address ways to identify the nodes that are part of the path in the mesh.

41. The arguments with respect to Thorson not disclosing system control processors that are interconnected via links is not persuasive because the cited text portion discloses processors elements that are interconnected via pathways **[col. 8 lines 34-37]**.

42. The argument with respect to there being no finding of a reasonable expectation of success is not persuasive because Thorson, Passint and the APA are all drawn to the same type of architecture, namely mesh architectures.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEFFREY M. RUTKOWSKI whose telephone number is (571)270-1215. The examiner can normally be reached on Monday - Friday 7:30-5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeffrey M Rutkowski
Patent Examiner
02/13/2009

/Hassan Kizou/
Supervisory Patent Examiner, Art Unit 2419